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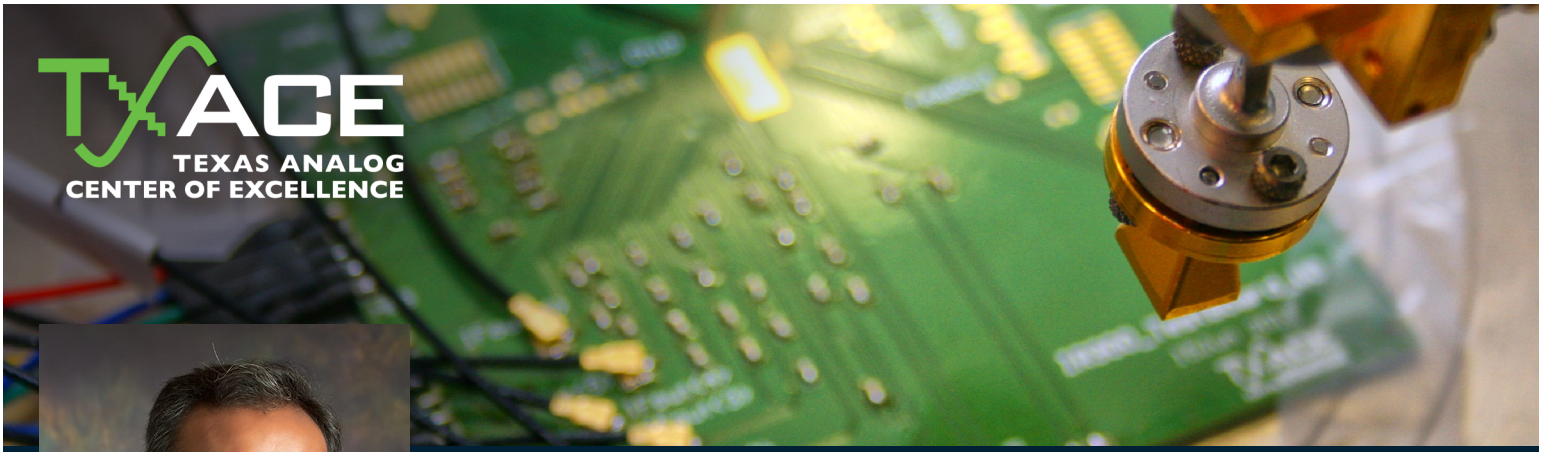

Ring-Oscillator Phase-Locked Loops for Beyond 100 Gb/s SerDes

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BIO

Pavan Hanumolu is a Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received a Ph.D. from the School of Electrical Engineering and Computer Science at Oregon State University in 2006, where he subsequently served as a faculty member until 2013. Dr. Hanumolu's research interests include energy-efficient integrated circuit implementation of analog and digital signal processing, frequency references, wireline communication systems, and power conversion. He served as the Editor-in-Chief of the IEEE Journal of Solid-State Circuits and an IEEE Fellow.

ABSTRACT

Multi-phase, low-noise clock synthesizers are essential for maximizing the performance of high-speed serial transceivers. Conventionally, these synthesizers rely on LC-oscillator-based phase-locked loops (PLLs). However, integrating multiple LC oscillators in a multi-lane transceiver and generating multiple phases within such systems have presented notable hurdles. Alternative solutions, such as ring oscillators (ROs), offer multiple phases but suffer from poor phase accuracy and heightened sensitivity to supply noise, particularly when pushed beyond 10 GHz frequencies.

In this eWorkshop, we explore methods to enhance the phase noise performance and supply noise immunity of RO-based PLLs operating at frequencies exceeding 10 GHz. Key design techniques are discussed, including implementing a type-III supply-regulated architecture to widen the frequency range and mitigate supply sensitivity. Moreover, a high-gain sampling phase detector is introduced to minimize in-band phase noise alongside a low-noise multiphase RO design to reduce out-of-band noise.

Experimental results from prototype PLLs fabricated using the Intel16 process demonstrate remarkable achievements. These include a wide operating range of 7 to 14 GHz and low noise levels greater than 70 fs r.m.s. jitter, and exceptional supply noise immunity exceeding 30 dB rejection. Through this seminar, attendees will gain insights into cutting-edge techniques for advancing the performance of multi-phase, low-noise RO-based clock synthesizers in high-speed serial transceiver applications.

Friday, April 26, 2024 at 1:00 – 2:00 p.m.
Osborne Conference Room (ECSS 3.503)

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