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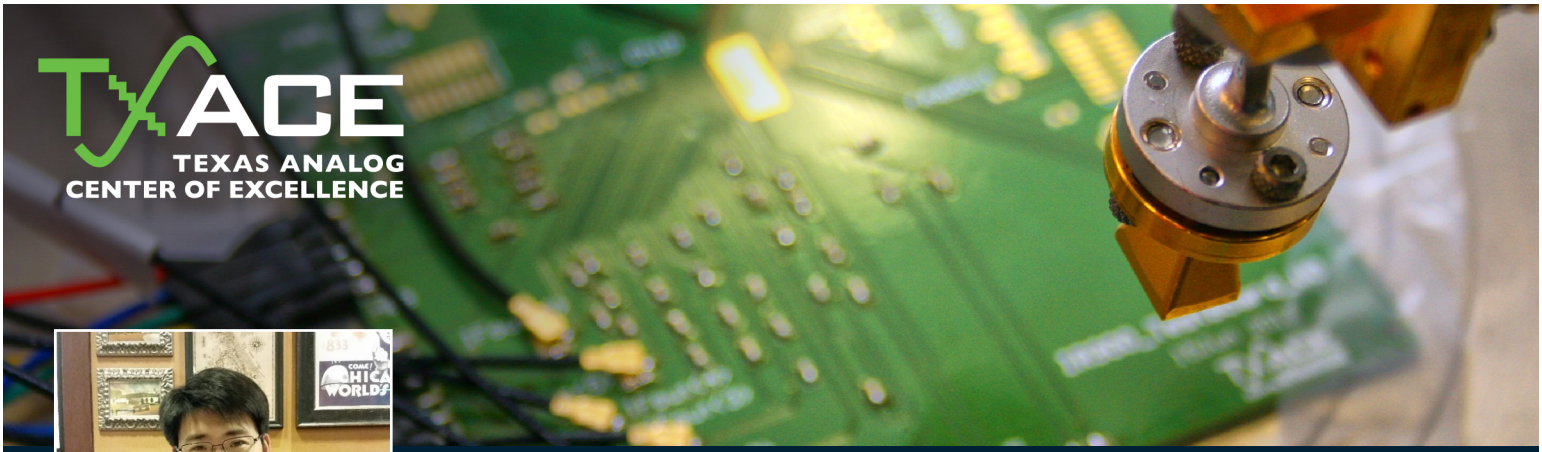

# Exploration of Proactive Power Management for Supply Droop Mitigation of Digital SoCs with Fully Integrated Power Converters


## Jie Gu

*Associate Professor*
*Northwestern University*


## BIO

Jie Gu is currently an associate professor in Northwestern University. He received his B.S. degree from Tsinghua University, M.S. degree from Texas A&M University and Ph.D. degree from University of Minnesota. From 2008 to 2010, he was an R&D engineer in Texas Instruments, Dallas, TX working on low voltage design and power management techniques for microprocessors in the smartphones. From 2011 to 2014, he was with Maxlinear developing mixed-signal broadband SoC chips. He joined ECE department of Northwestern University from 2015 with a research focus on novel circuit and architecture techniques for modern SoCs and machine learning accelerators. He is a recipient of NSF CAREER award.


## ABSTRACT

Maintaining power integrity has become increasingly challenging due to lower supply voltages in advanced CMOS technology and higher workload transients in modern digital processors. Conventional feedback-based power management scheme is often limited by the slow response time of the power converters while the use of advanced fast digital LDOs can cause additional efficiency loss. To mitigate such an issue, proactive droop management techniques offer attractive merits, e.g. faster response, advanced computing capability for complex chip conditions. In this talk, I will present our recent exploration of machine learning based proactive power management for supply droop mitigation with a fast fully-integrated buck converter. The 65nm test chip demonstrated that real-time prediction and reduction of supply droop from CPU activities can be achieved using an on-chip machine learning core and an integrated power converter. The proactive approach allows faster response from the power converters leading to up to 9% improvements on CPU performance or energy efficiency compared with conventional approaches.


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