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Powering Next-Gen SoCs: Innovations in High Conversion Ratio Voltage Converters and Design Approaches

Deukhyoun Heo

Partha Pratim Pande

ABSTRACT

The current technological landscape sees rapid advancements in areas like automotive vehicles, data centers, high-performance computing (HPC), and the Internet-of-Smart-Things (IoSTs). With the increasing adoption of high voltage rails to improve energy efficiency, there is a clear need for power management systems that can manage the significant voltage differences between input rails and load voltages. Addressing this, voltage regulators are evolving to offer high conversion ratios, essential to minimizing power distribution losses. Notably, embedded HPC systems, characterized by manycore architectures, present challenges due to significant power and temperature constraints. The traditional method of generating sub-1 V supply voltages for on-chip cores involves cascading multiple buck converters. This talk will outline the key challenges and potential solutions in power delivery, with an emphasis on High Conversion Ratio (HCR) hybrid converters for upcoming system-on-chips. Furthermore, we introduce a machine learning (ML) framework designed to optimize power delivery systems, capable of determining the best circuit parameters under specific design constraints, thus reducing design time and costs.

Deukhyoun Heo (presenter)

Professor
Washington State University

BIO

Deukhyoun Heo received his Ph.D. in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2000. That year, he joined the National Semiconductor Corporation. In Fall 2003, he joined the faculty of the School of Electrical Engineering and Computer Science at Washington State University, where he is now the Frank Brands Analog Distinguished Professor. He has authored about 200 publications, including 100 journal and 100 conference papers. Dr. Heo is a member of the IEEE MTT-S International Microwave Symposium Committee. He's been an associate editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —PART II and IEEE TRANSACTIONS ON MICROWAVE THEORY. He's an AE for IEEE TVLSI and MWTL and received the 2000 Best Paper Award from IEEE MTT-S IMS and the 2009 NSF CAREER Award.

Partha Pratim Pande

Professor
Washington State University

BIO

Partha Pratim Pande is a professor and holder of the Boeing Centennial Chair in computer engineering at the school of Electrical Engineering and Computer Science, Washington State University, Pullman, USA. He is currently the director of the school. His current research interests are novel interconnect architectures for manycore chips, on-chip wireless communication networks, heterogeneous architectures, and ML for EDA. Dr. Pande currently serves as the Editor-in-Chief (EIC) of IEEE Design and Test (D&T). He is on the editorial boards of IEEE Transactions on VLSI (TVLSI) and ACM Journal of Emerging Technologies in Computing Systems (JETC) and IEEE Embedded Systems letters. He was the technical program committee chair of IEEE/ACM Network-on-Chip Symposium 2015 and CASES (2019-2020). He also serves on the program committees of many reputed international conferences. He has won the NSF CAREER award in 2009. He is the winner of the Anjan Bose outstanding researcher award from the college of engineering, Washington State University in 2013. He is a fellow of IEEE.

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