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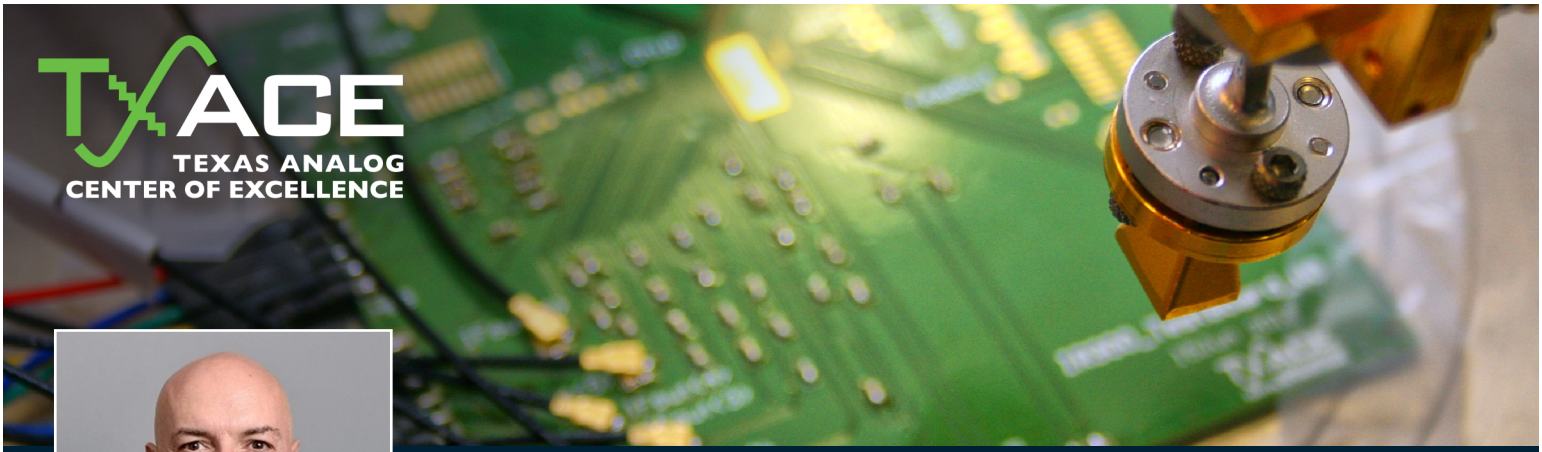

Digitally Enhanced, High Efficiency, Fast Settling Augmented DCD Converters

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BIO

Dr. Bakkaloglu received his PhD from Oregon State University in 1995 and joined Texas Instruments Inc. Mixed Signal Wireless Design Group, Dallas, TX, where he worked on system-on-chip designs with integrated battery management and RF, analog baseband functionality as a design leader. In 2004 he joined the Electrical Engineering Department at Arizona State University, Tempe, AZ. His current research interests include mixed signal circuit design for power supply regulators, sensor interface circuits, fractional-N frequency synthesizers, high speed A/D and D/A converters and built-in-self-diagnostic circuits for high reliability mixed signal circuits. Dr. Bakkaloglu has been associate editor for IEEE Transactions on Circuits and Systems and IEEE Transactions on Microwave Theory and Techniques. He was the General Chair for 2015 IEEE RFIC Symposium, and the founding chair of IEEE Solid State Circuits Society Phoenix Chapter. He is an IEEE Fellow and a Member of National Academy of Inventors.

ABSTRACT

State-of-the-art digital loads such as application processors, DSPs, FGPAs require a tight regulation window for its supply voltages after fast load transients. Recently, utilizing nonlinear control techniques and auxiliary circuits gain popularity due to their enhanced efficiency and design flexibility. In this SRC project, a current-mode DCDC buck converter with low-cost auxiliary stage utilizing a smaller inductor and a novel nonlinear control scheme for fast load transient response is developed. The proposed approach targets limiting the output voltage regulation window during fast load transient events. An auxiliary stage with a 100nH small inductor and the proposed Multiple-Single-Cycle-Non-Linear-Control (MSC-NLC) scheme operating with high switching rate shares the 100uF load capacitor with the main-stage. The main stage employs a 1uH inductor and operates with lower switching frequency of around 500kHz. Thereby, the main-stage provides high efficiency during steady-state power conversion operation while auxiliary-stage provides fast settling under fast-load-transients. Small-signal models (SFG model, Continuous-Time model and switching model) have been developed to investigate the popular control schemes for the main-stage, such as PWM, COT and hysteretic controls. The current-mode hysteretic control is selected for its fast response speed and easy implementation for stability. A second-order PLL based frequency synchronization circuit is introduced to lock the switching frequency at 500kHz for better EMI performance. Observer-based load capacitor current estimator is developed (called transient-detector) to implement the MSC-NLC that controls the auxiliary-stage to work as a Current-Controlled-Current-Source. Due to the large down-conversion ratio in this project (V_{in}=5V, V_{out}=0.5~0.8V), we further introduce braking-diode technique to significantly improve the negative step response and balance the step response symmetry. The benefits of the proposed control scheme include improved voltage droop/overshoot and settling time, easy analog computation for timing parameters, and a semi-closed-loop control to accommodate all non-idealities. The augmented buck converter is designed and fabricated in a 180nm BCD process with six levels metal routing. The converter IC occupies 2.5mm x 3mm, while the core controller area is only 0.8mm^2. The output voltage deviations with and without the auxiliary-stage and MSC-NLC shows that, for a specified output load capacitor, the maximum output voltage deviation is reduced by 3~4x.

Friday, January 20, 2023 at 1:00 – 2:00 p.m.
John von Neumann Room (ECSS 3.910)

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