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BIO

Visvesh Sathe is currently at the University of Washington where his group, the Processing Systems lab, works on a range of problems spanning energy efficient computing and integrated circuits for chronic bidirectional brain computer interfaces. Prior to joining UW, he spent six years at AMD where he invented and contributed to the translation of low power technologies into volume production. He currently serves on the IEEE SSCS webinar committee to promote professional and student development and is a distinguished lecturer of the IEEE Solid State Circuits Society, and in the Technical Program Committee of the Custom Integrated Circuits Conference and the International Solid-State Circuits Conference.

Regenerative Breaking: Recycling Energy from Duty-Cycled SoC Domains for Energy Minimization

ABSTRACT

SoCs domains in wearable and IoT applications are frequently duty-cycled, placed in a power-gated (*Sleep*) mode, and only woken up for brief periods to periodically perform tasks. Duty cycling reduces steady-state leakage energy loss, but the significant quantity of energy stored in the domain decoupling capacitor at the onset of *Sleep* mode is discharged through domain leakage. This energy overhead significantly degrades overall system efficiency in such systems.

In this talk, we will present a power delivery architecture that reverses power flow from the load back to the power source to recycle the otherwise wasted electrical energy. We will observe that recovering too much or too little energy are both sub-optimal, motivating a computationally guided approach to recover an optimal quantity of stored energy, one that minimizes the overall losses in the system. Test-chip measurements of a duty-cycled, buck-regulated ARM M0 processor used to demonstrate the effectiveness of Regenerative Breaking in 65nm CMOS will be discussed. The talk will also include a discussion into some of the limitations of our approach.

Friday, June 24, 2022 at 1:00 – 2:00 p.m.
Osborne Conference Room (ECSS 3.503)