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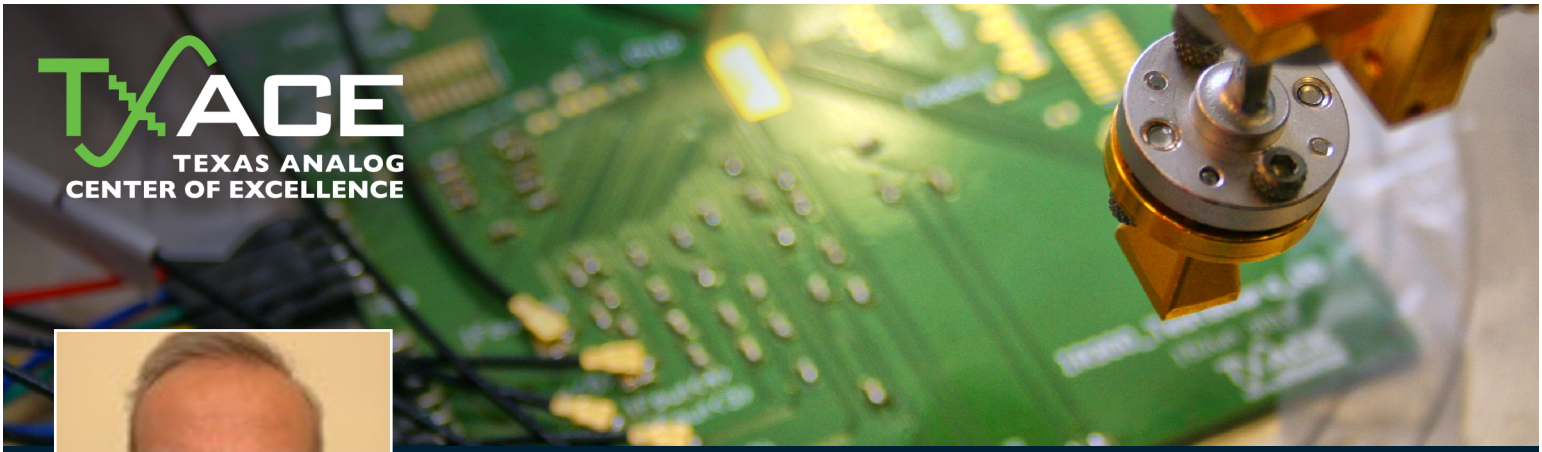

Machine Learning Driven Automatic Mixed-Signal Design Validation: Pre Through Post-Silicon

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BIO

Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech and a Fellow of the IEEE. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Dr. Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received seven Best Paper Awards and three Best Paper Award nominations. His work on self-healing chips was featured as one of General Electric's key technical achievements in 1992 and was cited by the *Wall Street Journal*. In 1995, he was named a Collaborating Partner in NASA's New Millennium project. In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. In 2007, his group received the Margarida Jacome Award for work on VIZOR: Virtually Zero Margin Adaptive RF from the Berkeley Gigascale Research Center (GSRC). Dr. Chatterjee has authored over 450 papers in refereed journals and meetings and has 22 patents. He is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as chairman and chief scientist from 2000-2002. His research interests include error-resilient signal processing and control systems, mixed-signal/RF/multi-GHz design and test and adaptive real-time systems.

ABSTRACT

Top-down design transformation from behavioral models to transistor netlists to physical layout consists of iterative refinement of the parameters of the component models in a hierarchical manner until the design parameters at the transistor netlist and physical layout of the system are optimal. Throughout this process, discrepancies between input-output behavior as predicted by higher level models vs. low level design descriptions need to be detected and debugged at each step and may arise from modeling errors (including process variability effects) or unknown design bugs. Consequently, the debugging technique cannot be predicated on assumed design bug models; the bugs need to be discovered and modeled during design debug itself. To address these issues, we develop collaborative test generation and behavior learning algorithms for detection of behavioral discrepancies between high level behavioral design descriptions (AHDL) and low level (netlist, silicon) module implementations across the entire stimulus space of the design. The methodology can be applied through different stages of design evolution, pre as well as post-silicon. Application to a diverse range of mixed-signal circuit types is demonstrated through simulation experiments and hardware measurements. Further, a signature-matching design of experiments approach is proposed for diagnosing design bugs to individual circuit modules in a probabilistic manner. A ranking of likely buggy modules is produced that is shown to be very accurate across bug diagnosis studies performed on a variety of mixed-signal circuits.

Friday, April 22, 2022 at 1:00 – 2:00 p.m.
Osborne Conference Room (ECSS 3.503)

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