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Generating Current Constraints for Electromigration Safety

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BIO

Farid N. Najm is a Professor with the Department of Electrical and Computer Engineering (ECE) at the University of Toronto. He has a B.E. degree in Electrical Engineering from the American University of Beirut (AUB) and a Ph.D. degrees in ECE from the University of Illinois at Urbana-Champaign (UIUC) in 1989. He worked with Texas Instruments in Dallas, TX, 1989-1992, then joined the ECE Department at UIUC as an Assistant Professor, becoming Associate Professor in 1997. In 1999, he joined the ECE Department at the University of Toronto, where he became Professor in 2001, then served as Vice-Chair from 2004 to 2007 and as Department Chair from 2009 to 2019.

Dr. Najm is a Fellow of the IEEE and a Fellow of the Canadian Academy of Engineering. He was Associate Editor for the IEEE Transactions on CAD 2001-2009. He received the IEEE Transactions on CAD Best Paper Award in 1992, the NSF Research Initiation Award in 1993, the NSF CAREER Award in 1996, and was Associate Editor for the IEEE Transactions on VLSI 1997-2002. He served as General Chairman for the 1999 ISLPED and as Technical Program Co-Chairman for ISLPED-98. He has also served on the technical committees of ICCAD, DAC, CICC, ISQED, and ISLPED. His work has been recognized the DAC prolific author award in 2013 and the ICCAD best paper awards in 2016, 2019 and 2020. Dr. Najm has authored the text Circuit Simulation, John Wiley & Sons, 2010. His research is on computer-aided design (CAD) for integrated circuits, with an emphasis on circuit level issues related to power dissipation, timing, and reliability.

ABSTRACT

Electromigration (EM) remains an important failure mechanism in integrated circuits, in spite of several decades of research and development. With the increased density and functionality of modern integrated circuits, EM in the on-die power/ground grid is an especially challenging problem. This project is focused on generating constraints that the supply currents drawn by the underlying circuit blocks must satisfy in order to guarantee EM safety in the on-chip power grid. This safety is based on an accurate physical model of EM that comprehends atomic flux and material flow among connected metal lines. Normally, one takes user-provided currents as inputs and produces the stress in metal lines as output, and this forms the basis for EM checking and verification. In contrast, we are solving what may be called the inverse problem: given a grid and a safety threshold for stress in the metal lines, we want to produce constraints on the circuit supply currents that guarantee EM safety. These constraints, taken altogether, provide a description of the space of safe currents, which we call the safety set.

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