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Single-Inductor Multiple Output (SIMO) Voltage Regulators for Energy Efficient SoCs: Challenges, Observations and Recent Advances

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BIO

Visvesh S. Sathe received the B.Tech. degree from the Indian Institute of Technology, Bombay and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor. He is currently an Associate Professor of Electrical and Computer Engineering at the University of Washington where he leads the Processing Systems Lab (PSyLab), focused on research associated with energy-efficient computing and implantable electronics. Prior to joining the University of Washington, he served as a Member of Technical Staff in the Low-Power Advanced Development Group at AMD, where his research focused on inventing and implementing circuit, clocking and supply mitigation technologies in next-generation microprocessors. These technologies include high-speed digital circuits, adaptive clocking for supply noise mitigation and resonant clocking. His current research interests include implementation of run-time hardware control and optimization in digital and mixed-signal systems over a range of applications. He is the recipient of an NSF Career award in 2019 and more recently the Intel outstanding researcher award in 2021. He serves on the technical program committee of the IEEE Custom Integrated Circuits Conference and as a Distinguished Lecturer of the SSCS

ABSTRACT

Fine-grained voltage control of SoC domains remains a salient mechanism for energy efficient design. Single-Inductor Multiple-Output (SIMO) converters are a promising technology for enabling fine-grained supply voltage (Vdd) domains in SoCs. With efficiencies approaching those of buck converters, SIMO regulators allow multiple domains to share a single inductor, thus reducing the use of bulky passive components. However, these regulators suffer from poor transient response and significant ripple, requiring extensive Vdd margining. Operating at an elevated Vdd, and therefore load-current, inflates power draw and further reduces system efficiency. In this seminar, we describe some of the challenges associated with SIMO regulation, including their impact on overall SoC efficiency. We describe two recent techniques to address these challenges: Dynamic Droop Allocation (DDA) through concurrent domain-Vdd control, and adaptive clocking using the UniCap architecture. We demonstrate the effectiveness of both techniques on anintegrated 4-domain SIMO System on Chip (SoC) in 65nm CMOS. Measurements indicate that compared to conventional SIMO implementations, Vdd guard-band reductions obtained by UniCaP(98%) and DDA(40%) reduce total system power draw by 53% and 31% respectively. We conclude by sharing our perspective on the challenges that need to be addressed by SIMO regulator design before their broader adoption in real-world SoCs be-comes more attractive.

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Virtual Seminar

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