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The Crystal Ball for Chip Design

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ABSTRACT

Chip design is so complex and its productivity has long been restricted by the challenge of design prediction. That is, the impact of early designs steps on final products is huge yet immensely difficult to predict. Conventional approaches of design predictions are either impractically expensive to use or insufficiently accurate. Machine learning, by knowledge extraction from data and reuse, offers an opportunity to overcome this challenge. This presentation introduces machine-learning techniques for fast and credible predictions of rout ability, crosstalk, net-length and analog circuit performance. In general, machine-learning applications tend to be plug-in use with parameter tuning and therefore their advantages are not fully utilized for specific problems. To this end, we show how to customize machine learning architectures by leveraging domain knowledge so that inference accuracy is further improved.

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BIO

Jiang Hu is currently a professor in the Department of Electrical and Computer Engineering at Texas A&M University. His research interests include design and automation of VLSI circuits and systems, computer architecture optimization and hardware security. He has published over 200 technical papers. He received a best paper award at the ACM/IEEE Design Automation Conference (DAC) in 2001, an IBM Invention Achievement Award in 2003, a best paper award at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) in 2011 and a best paper award at the IEEE International Conference on Vehicular Electronics and Safety in 2018. He served as an associate editor for the IEEE Transactions on CAD from 2006 to 2011, and currently serves as an associate editor for the ACM Transactions on Design Automation of Electronic Systems. He was the technical program chair and the general chair of the ACM International Symposium on Physical Design (ISPD) in 2011 and 2012, respectively. He has also served in the technical program committees of numerous conferences and symposiums including DAC, ICCAD, ISPD, ISLPED, DATE, ASP-DAC, ICCD, ISQED, ISCAS and GLSVLSI. He received the Humboldt Research Fellowship in 2012 and was named an IEEE fellow in 2016 .

Yiran Chen

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BIO

Yiran Chen received B.S (1998) and M.S. (2001) from Tsinghua University and Ph.D. (2005) from Purdue University. After five years in industry, he joined University of Pittsburgh in 2010 as Assistant Professor and then promoted to Associate Professor with tenure in 2014, held Bicentennial Alumni Faculty Fellow. He is now the Professor of the Department of Electrical and Computer Engineering at Duke University and serving as the director of NSF Industry–University Cooperative Research Center (IUCRC) for Alternative Sustainable and Intelligent Computing (ASIC). He is the co-director of Duke Center for Computational Evolutionary Intelligence (CEI), focusing on the research of new memory and storage systems, machine learning and neuromorphic computing, and mobile computing systems. Dr. Chen has published one book and more than 400 technical publications and has been granted 96 US patents. He serves or served the associate editor of more than ten international academic transactions/journals and served on the technical and organization committees of more than 60 international conferences. He is now serving as the Editor-in-Chief of the IEEE Circuits and Systems Magazine. He received seven best paper awards, one best poster award, and fourteen best paper nominations from international conferences and workshops. He is the recipient of the NSF CAREER award, the ACM SIGDA outstanding new faculty award, the Humboldt Research Fellowship for Experienced Researchers, and the IEEE SYSC/CEDA TCCPS Mid-Career Award. He is a distinguished lecturer of IEEE CEDA and listed in the HPCA Hall of Fame. He is a Fellow of the ACM and IEEE.

Friday, January 22, 2021 at 1:00 – 2:00 p.m.
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