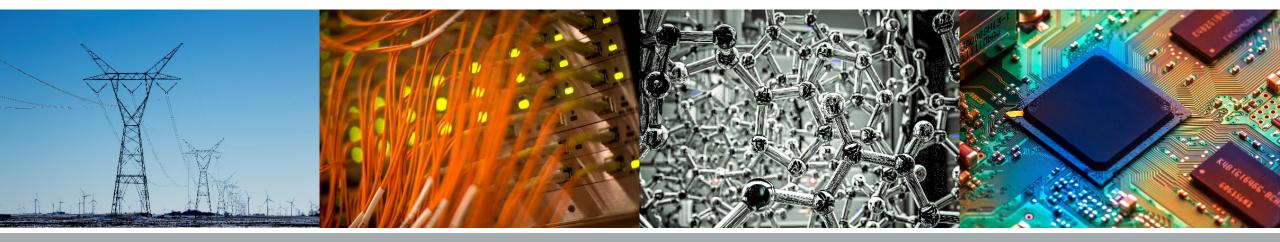
Integrated Circuit Design in the Deep Learning Era

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Organizers

Pavan Hanumolu & Naresh R. Shanbhag

Electrical & Computer Engineering COLLEGE OF ENGINEERING

Objective

- Deep learning (DL) has proven to be enormously successful in solving problems previously thought to be intractable in a diverse set of domains.
- This panel explores the potential and applicability of DL-based techniques in the **integrated circuit (IC) design** space. Specifically, the panel features experts from both industry and academe who will share their thoughts.

Panelists

Todd Younkin President and CEO, SRC







Tanay Karnik Principal Engineer & Director, Intel Labs

Mahesh Mehendale TI Fellow, Kilby Labs

Naveen Verma Professor, Princeton University

ILLINOIS Electrical & Computer Engineering COLLEGE OF ENGINEERING

Topic 1 - DL in Design Automation

- What role can DL methods play/are playing in enhancing **IC design methodologies** today?
 - What role does DL play in electronic design automation and IC testing today and what are its future prospects?
 - Will DL approaches be effective in reducing design effort and increase productivity? Or will its hard-to-interpret outcomes and unpredictability make it an unsuitable tool?
 - Will data-driven methods make analog/RF/IC designers obsolete?

Topic 2 – Design of ICs for DLs

- In the design of ICs for DL, have any fundamentally new design techniques or concepts been discovered or is it mainly the case of an "old technology with new terminology"?
 - spatial architectures essentially a throwback to systolic arrays circa 1978 [H. T. Kung]?
 - compute kernels such as convolutions and MVM, and their fast implementations, have been well-studied in other disciplines, e.g., DSP and communications. What's new?
 - DL workloads are eminently parallelizable so what is the challenge?
 - if hardware is essentially a rehash or old techniques, is the novelty in software and applications-to-architecture mapping?
 - are in-memory architectures (IMCs) the 'true' novel aspect of hardware for DL? what are its limitations?

Topic 3 – DL-assisted ICs and Systems

- What is the potential for DL-assisted integrated circuits and systems?
 - we know DL works best when the statistical structure of data is complex and unknown (ImageNet) or when the algorithmic structure of a task is complex (Go games). Where are such opportunities in integrated circuits and systems?
 - AFE's in communication links are routinely calibrated in a data-driven manner. Is this an opportunity for insertion of DL-based methods?
 - is there a role for DL in the algorithmic/circuit side of signal processing and communication systems?

Topic 4 – Impact of DL on Career Opportunities

- What is impact of DL on career opportunities in the semiconductor area for both undergraduate and graduate students?
 - how do we adapt our pedagogy to prepare our students to be effective contributors in the DL era? How do we manage core vs. emerging topics in university curriculums?
 - how can the semiconductor industry prepare itself to 'receive' and nurture this new generation of DL aware/capable IC and system design engineers?
 - what role should the semiconductor industry play in the DL era? How can it be in the driver's seat?

Thank You!