# Integrated Circuit Design in the Deep Learning Era

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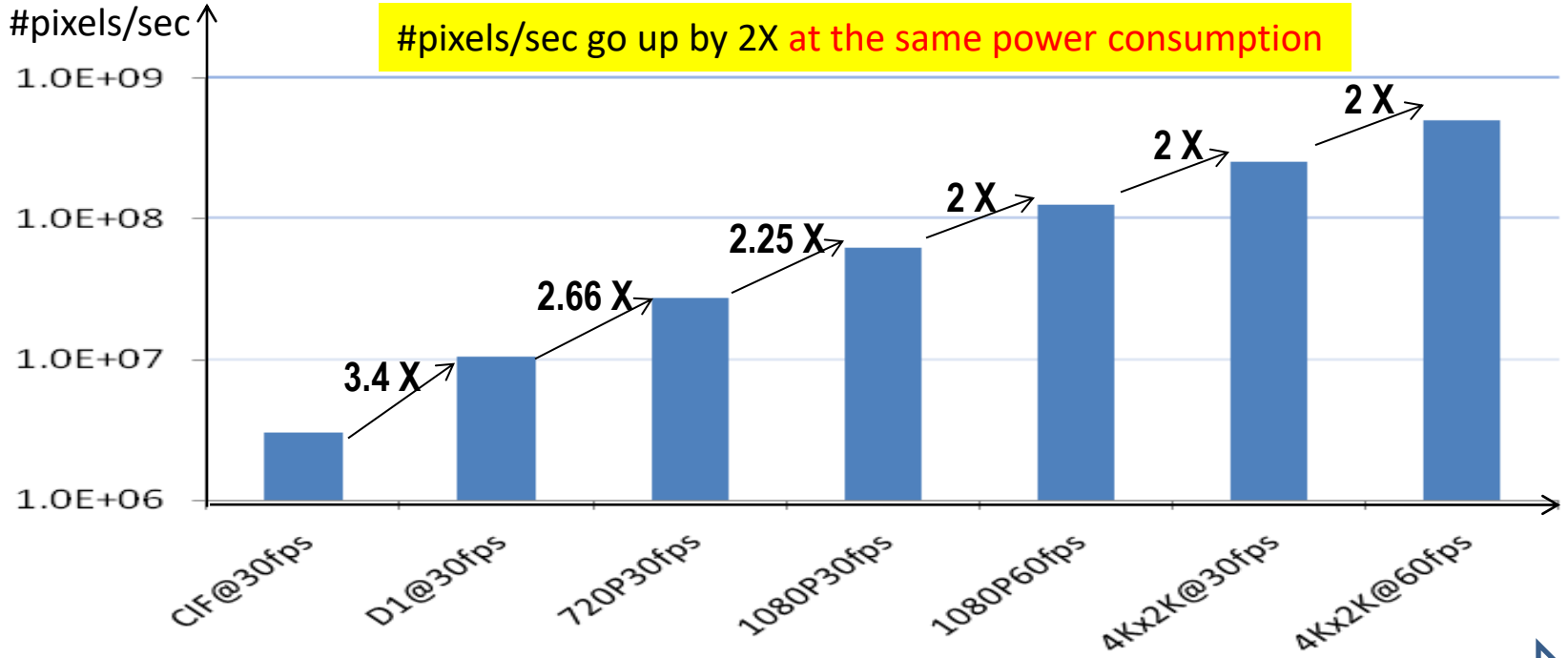
# Video Compression in Mobile Platforms




| | | | | | | |
|---|---|---|---|---|---|---|
| **Video Standard** | MPEG2 | MPEG4 | H.264 (BP) | H.264 (HP) | | HEVC |
| **Technology** | | 90nm | 65nm | 45nm | 28nm | … |
| **Architecture** | DSP | DSP+HWA | | HWA | HWA with highly // | ….?? |

# ML@Edge:
# what can we leverage but what's different?

- Started with HWAs while algorithms to be mapped evolving in parallel
  - makes it difficult to strike the efficiency vs configurability balance
- Technology scaling slowing down
  - need to focus more on circuits and architecture level optimizations
- Core compute less diverse and parallelizable
  - Higher leverage of super-optimized building blocks such as CiM macros
- No standards
  - Opportunity for system-algorithm-architecture-circuit level co-design
  - Makes it challenging to develop hardware to cater to a range of algorithms/systems
- Present focus on inferencing but "Learning@Edge" use-cases will emerge

# Thank you...