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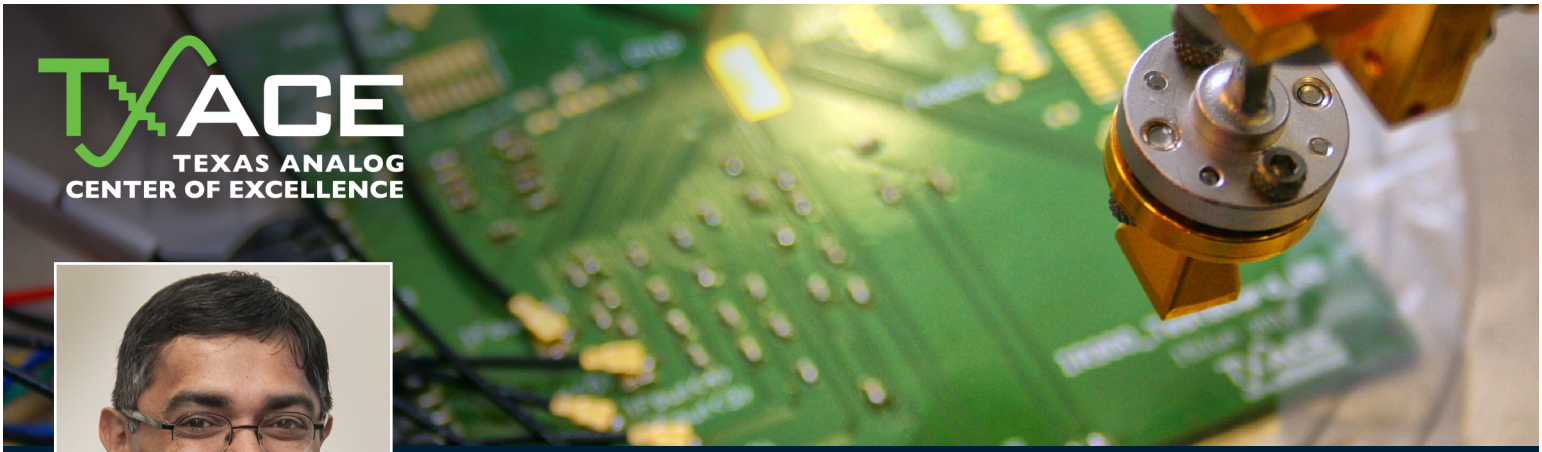

# Automated Layout of Analog Arrays in Advanced Technology Nodes


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## BIO

Sachin S. Sapatnekar received the Ph.D. degree from the University of Illinois at Urbana-Champaign in 1992. He teaches at the University of Minnesota, where he holds the Distinguished McKnight University Professorship and the Henle Chair Professorship in ECE. His research develops CAD techniques for the analysis and optimization of circuit performance, currently focused on analog and digital CMOS circuits. He is a recipient of twelve conference Best Paper Awards, the SRC Technical Excellence Award, and the SIA University Research Award. He is a Fellow of the IEEE and the ACM.


## ABSTRACT

Numerous analog circuits rely on the design of well-matched arrays of passive and active devices. The considerations in designing these arrays include the ability to handle potentially conflicting factors: matching and resilience to systematic/random process variations, compact layout, low-parasitic routing, and thermal, electromigration, and IR drop constraints on wires that can degrade performance. Particularly in recent technology nodes (FinFET and beyond), this has become a major challenge. This talk describes efforts in developing methods that automate the design of these structures, considering both metrics local to the array and metrics that capture their impact on the performance of larger circuits that use these arrays. Methods for building common-centroid layouts for capacitive and transistor arrays will be described, as well as an analysis to determine the appropriate use of the graded use of matching in common-centroid and interdigitated layouts, depending on the sensitivity of the circuit to layout-dependent variations.


Friday, August 25, 2023 at 1:00 – 2:00 p.m.
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