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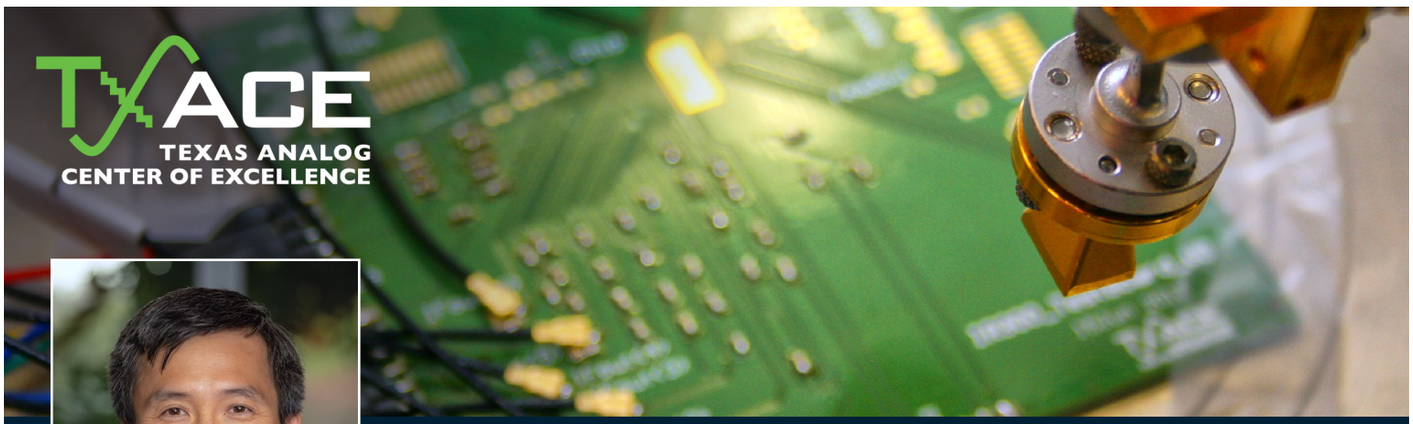

Two-Stage Vertical Power Delivery and Management for Efficient High-Performance Computing

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BIO

Dr. Hanh-Phuc Le is an Assistant Professor of ECE at the University of California San Diego and a co-Director of the Power Management Integration Center, an NSF IUCRC center. He received the Ph.D. degree from UC Berkeley (2013), M.S. from KAIST, Korea (2006), and B.S. from Hanoi University of Science and Technology in Vietnam (2003), all in Electrical Engineering. In 2012, he co-founded and served as the CTO at Lion Semiconductor until October 2015. The company was acquired by Cirrus Logic in 2021. He was with the University of Colorado Boulder from 2016 to 2019, before joining the ECE department at UC San Diego. He held R&D positions at Oracle, Intel, Rambus, JDA Tech in Korea and the Vietnam Academy of Science and Technology (VAST) in Vietnam. His current research interests include miniaturized/on-die power conversions, large conversion ratios, smart power delivery and control for high performance IT systems, data centers, telecommunication, robots, automotive, mobile, wearable, and IoT applications.

Dr. Le received a 2021 NSF CAREER Award, a 2012-2013 IEEE Solid-State Circuits Society Pre-doctoral Achievement Award, and UC Berkeley's 2013 Sevin Rosen Funds Award for Innovation. He authored three book chapters, over fifty journal and conference papers with one best paper award in various topics in the area of integrated power electronics. He is an inventor with 22 U.S. patents (12 granted and 10 pending). He serves as an associate editor of the IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE), TPC Chair/co-chair for the International Workshop on Power Supply On Chip (PwrSoC 2018, 2020), Chair of the Power Management and Outreach Subcommittees at the IEEE Custom Integrated Circuits Conference (2020, 2021), and Vice Chair of the Energy Conversion Congress and Exposition (ECCE) 2021 and 2022. He is also the Chair of the IEEE Power Electronics Society Technical Committee on Power Components, Integration, and Power ICs (IEEE PELS TC2). Dr. Le is an IEEE Senior Member.

ABSTRACT

Emerging high-performance computing needs in data centers, autonomous vehicles, and mobile devices demand increasingly large peak currents at scaled-CMOS-compatible voltages (<1V). To ease otherwise high I2R losses in power delivery, most applications now target high system-level voltage busses (e.g., 20-60V) prior to arriving at the chip. However, incompatibility with scaled CMOS voltages means that DC-DC conversion must occur off-chip. State-of-the-art solutions tend to perform this via a PMIC located laterally away from the processor, which leads to large lateral losses and heat dissipation and, more importantly, requires a very large number of power pins. This is increasingly problematic for emerging AI/ML applications that require pin-intensive high-throughput memory access via highly-parallelized memory interfaces. While some recent work on integrated voltage regulators have attempted to place the second stage DC-DC converter physically closer to the processor to reduce lateral losses, the voltage seen by the die and/or within the package substrate is still around ~1.8V, which limits achievable C4 bump reduction of the overall approach. More importantly, traditional buck converters are utilized, which limits achievable efficiencies given physical resistance limitations of small inductors.

In this project, we propose to re-work conventional power delivery and management (PDM) approaches in a way that converts voltage down to <1V levels at the last and shortest possible distance, enabling significant savings in losses, thermal dissipation, and the required pin count for PDM. Specifically, we propose a 2-stage vertical PDM architecture combining a 4-to-1 switched-capacitor voltage regulator (SCVR) stage located within the package substrate, right underneath the processing die, along with a hybrid voltage regulator module (HVRM) stage located on the PCB. In this talk, the speaker will provide detail information of the architecture, technologies, circuit techniques, and fresh experimental results of the first generation prototype.

Friday, August 19, 2022 at 1:00 – 2:00 p.m.
Osborne Conference Room (ECSS 3.503)

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